300mA,Ultra-low noise, Small Package Ultra-Fast CMOS LDO Regulator

General Description

The LP3982 is designed for portable RF and wireless applications with demanding performance and space requirements. The LP3982 performance is optimized for battery-powered systems to deliver ultra low noise and low quiescent current. A noise bypass pin is available for further reduction of output noise. Regulator ground current increases only slightly in dropout, further prolonging the battery life. The LP3982 also works with low-ESR ceramic capacitors, reducing the amount of board space necessary for power applications, critical in hand-held wireless devices. The LP3982 consumes less than 0.01μA in shutdown mode and has fast turn-on time less than 50μs. The other features include ultra low dropout voltage, high output accuracy, current limiting protection, and high ripple rejection ratio. Available in the 5-lead of SC-70 packages.

Features

- Ultra-Low-Noise for RF Application
- 2V- 6V Input Voltage Range
- Low Dropout : 220mV @ 300mA
- 1.2V, 1.5V, 1.8V, 2.5V, 2.8V 3.0V and 3.3V Fixed
- 300mA Output Current, 550mA Peak Current
- High PSSR:-75dB at 1KHz
- < 0.01uA Standby Current When Shutdown
- Available in SC-70-5 Package
- TTL-Logic-Controlled Shutdown Input
- Ultra-Fast Response in Line/Load transient
- Current Limiting and Thermal Shutdown Protection
- Quick start-up (typically 50uS)

Applications

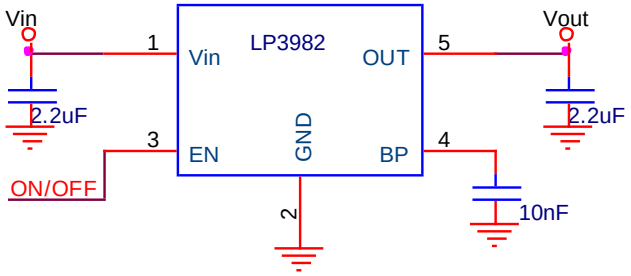
- Portable Media Players/MP3 players
- Cellular and Smart mobile phone
- LCD
- DSC Sensor
- Wireless Card

Order Information

LP3982 □ □ □ □ □ □

- F: Pb-Free
- Package Type
  - J5: SC-70
- Output Voltage Type
  - 12: 1.2V
  - 18: 1.8V
  - 25: 2.5V
  - 28: 2.8V
  - 30: 3.0V
  - 33: 3.3V
- Output Quick Recharge
  - Default: Not

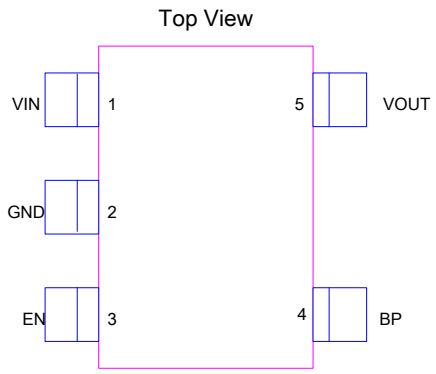
Typical Application Circuit



Marking Information

Device	Marking	Package	Shipping
LP3982			

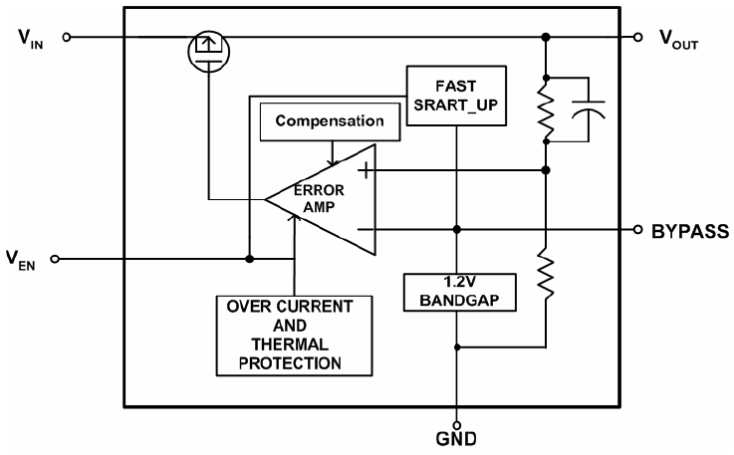
Functional Pin Description

Package Type	Pin Configurations
SC-70	

Pin Description

Pin	Name	Description
1	VIN	Power Input Voltage
2	GND	Ground
3	EN	Chip Enable (Active High). Note that this pin is high impedance.
4	BP	Reference Noise Bypass
5	VOUT	Output Voltage

Function Diagram



Absolute Maximum Ratings

- ✧ Supply Input Voltage ---------- 6V

Power Dissipation, PD @ TA = 25°C

- ✧ SC-70 ---------- 400mW

Package Thermal Resistance

- ✧ SC-70, θJA ---------- 250°C/W
- ✧ Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- ✧ Storage Temperature Range ---------- −65°C to 165°C

ESD Susceptibility

- ✧ HBM (Human Body Mode) ---------- 2kV
- ✧ MM(Machine-Mode) ---------- 200V

Recommended Operating Conditions

- ✧ Supply Input Voltage ---------- 2.5V to 5.5V

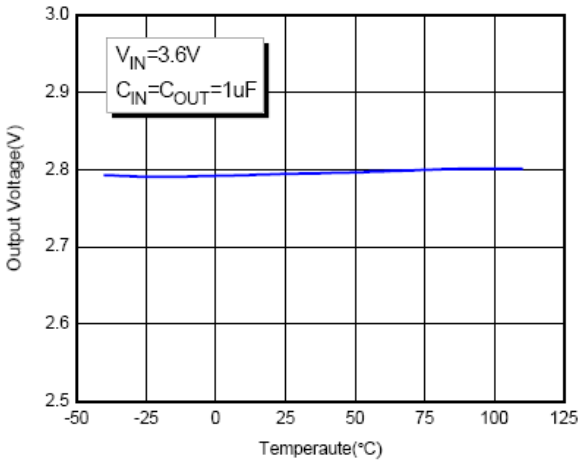
Electrical Characteristics

(VIN = VOUT + 1V, CIN = COUT = 1μF, , TA = 25° C, unless otherwise specified)

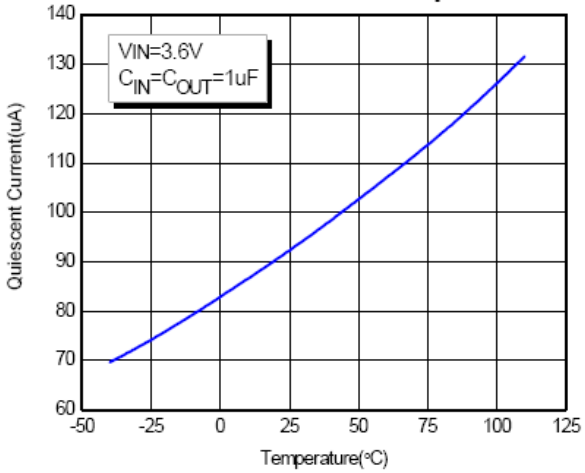
Parameter		Symbol	Test Conditions	Min	Typ	Max	Units
Output Voltage Accuracy		ΔV_{OUT}	I_{OUT} = 1mA	−2	--	+2	%
Current Limit		I_{LIM}	R_{LOAD} = 1Ω	300	400		mA
Quiescent Current		I_Q	V_{EN} ≥ 1.2V, I_{OUT} = 0mA		75	130	μA
Dropout Voltage		V_{DROP}	I_{OUT} = 200mA, V_{OUT} > 2.8V		170	200	mV
			I_{OUT} = 300mA, V_{OUT} > 2.8V		220	300	mV
Line Regulation		ΔV_{LINE}	V_{IN} = (V_{OUT} + 1V) to 5.5V, I_{OUT} = 1mA			0.3	%
Load Regulation		ΔV_{LOAD}	1mA < IOUT < 300mA			2	%
Standby Current		I_{STBY}	V_{EN} = GND, Shutdown		0.01	1	μA
EN Input Bias Current		I_{IBSD}	V_{EN} = GND or V_{IN}		1	5	uA
EN Threshold	Logic-Low Voltage	V_{IL}	V_{IN}=3V to 5.5V, Shutdown			0.4	V
	Logic-High Voltage	V_{IH}	V_{IN}=3V to 5.5V, Start-Up	1.2			V
Output Noise Voltage			10Hz to 100kHz, I_{OUT}=200mA C_{OUT}=1μF		100		uVRMS
Power Supply Rejection Rate	f=100Hz	PSRR	C_{OUT}=1μF, I_{OUT}=10mA		−75		dB
	f=10kHz				−65		dB
Thermal Shutdown Temperature		T_{SD}			150		°C

Typical Operating Characteristics

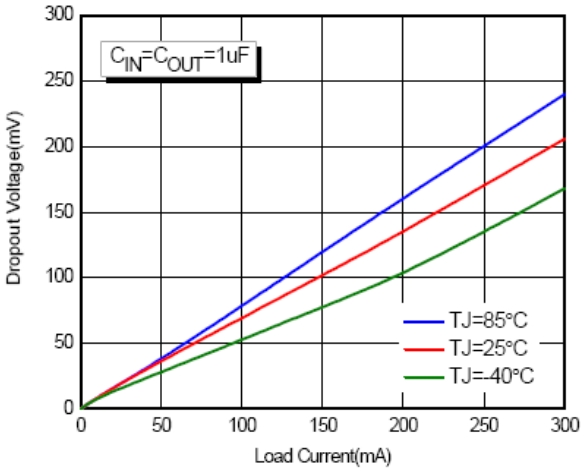
Output Voltage vs. Temperature



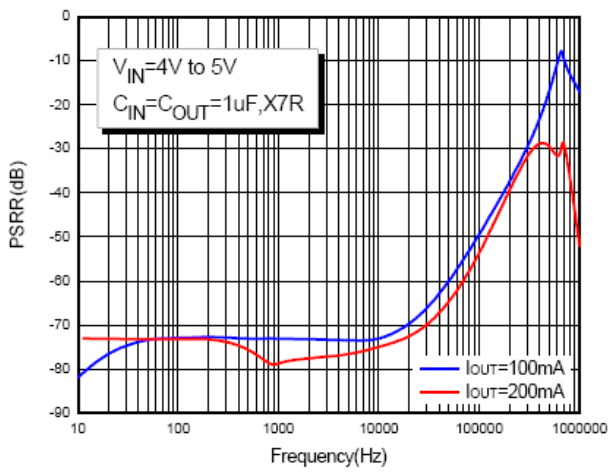
Quiescent Current vs. Temperature



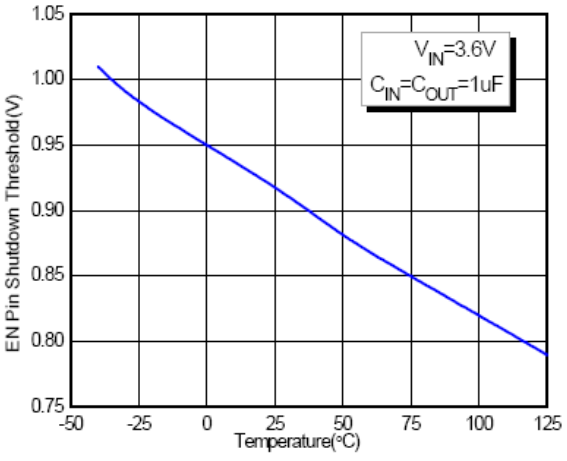
Dropout Voltage vs. Load Current



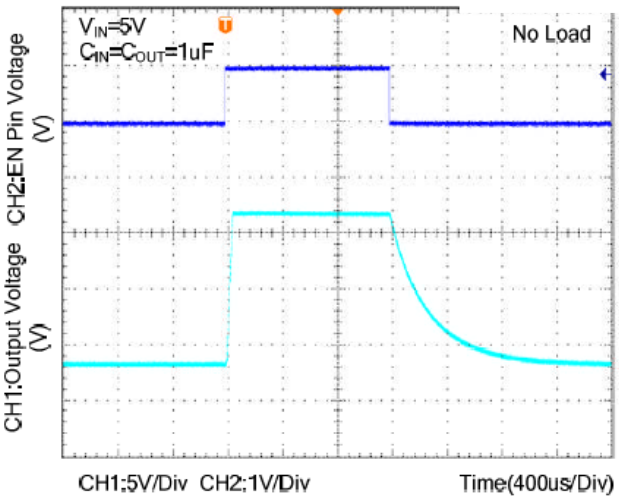
PSRR



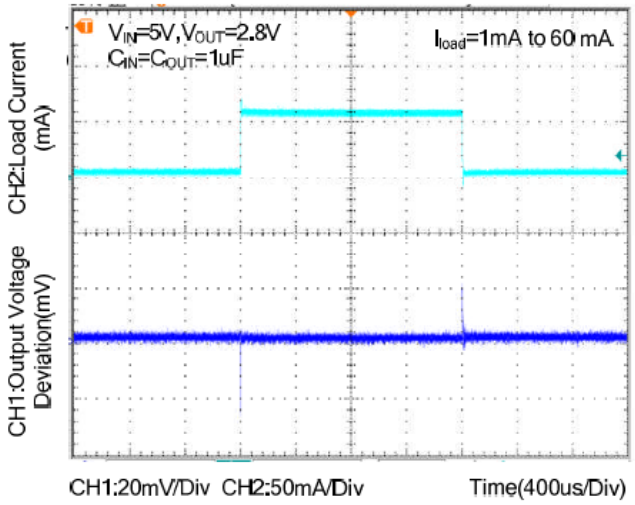
EN Pin Shutdown Threshold vs. Temperature



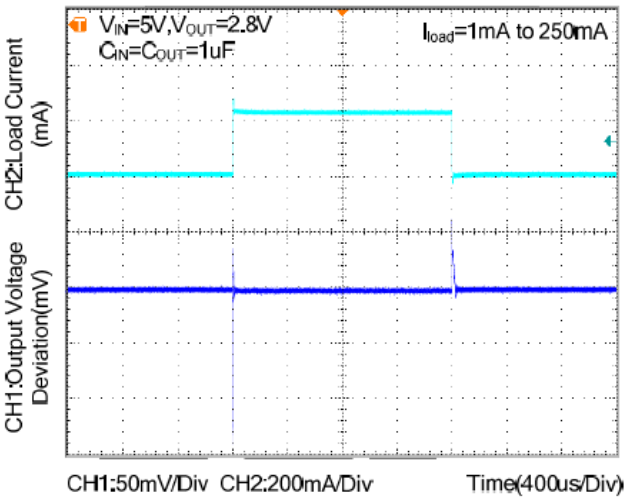
EN Pin Shutdown Response



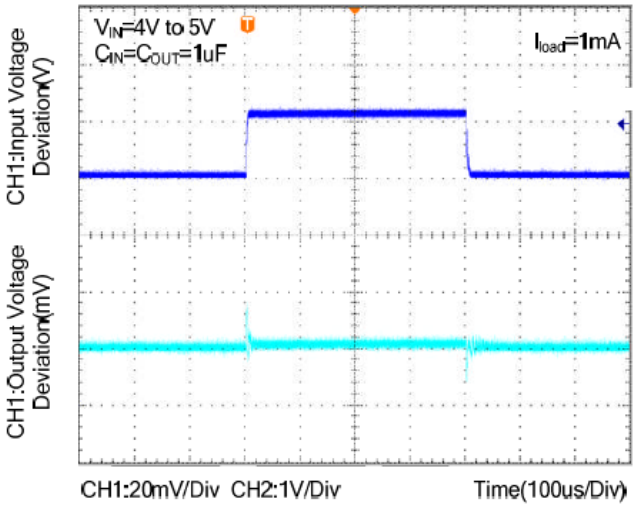
Load Transient Response



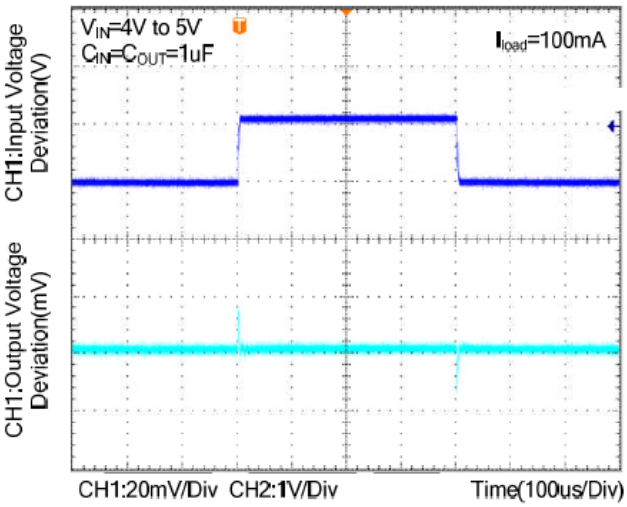
Load Transient Response



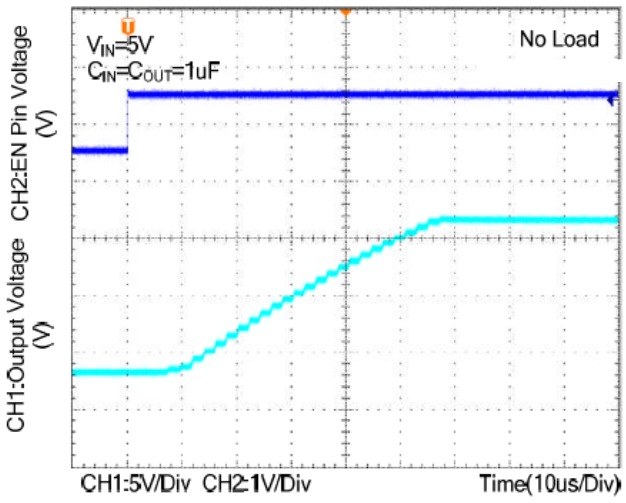
Line Transient Response



Line Transient Response



Start Up



Applications Information

Like any low-dropout regulator, the external capacitors used with the LP3982 must be carefully selected for regulator stability and performance. Using a capacitor whose value is > 1μF on the LP3982 input and the amount of capacitance can be increased without limit. The input capacitor must be located a distance of not more than 0.5 inch from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response. The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The LP3982 is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least 1μF with ESR is > 25mΩ on the LP3982 output ensures stability. The LP3982 still works well with output capacitor of other types due to the wide stable ESR range. Figure 1 shows the curves of allowable ESR range as a function of load current for various output capacitor values. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located not more than 0.5 inch from the VOUT pin of the LP3982 and returned to a clean analog ground.

Start-up Function Enable Function

The LP3982 features an LDO regulator enable/disable function. To assure the LDO regulator will switch on, the EN turn on control level must be greater than 1.2 volts. The LDO regulator will go into the shutdown mode when the voltage on the EN pin falls below 0.4 volts. For to protecting the system, the LP3982 have a quick-discharge function. If the enable function is not needed in a specific application, it may be tied to VIN to keep the LDO regulator in a continuously on state.

Bypass Capacitor and Low Noise

Connecting a 10nF between the BP pin and GND pin significantly reduces noise on the regulator output, it is critical that the capacitor connection between the BP pin and GND pin be direct and PCB traces should be as short as possible. There is a relationship between the bypass capacitor value and the LDO regulator turn on time. DC leakage on this pin can affect the LDO regulator output noise and voltage regulation performance.

Thermal Considerations

Thermal protection limits power dissipation in LP3982. When the operation junction temperature exceeds 150°C, the OTP circuit starts the thermal shutdown function turn the pass element off. The pass element turns on again after the junction temperature cools by 25°C. For continue operation, do not exceed absolute maximum operation junction temperature 125°C.

The power dissipation definition in device is :

$$PD = (VIN-VOUT) \times IOUT + VIN \times IQ$$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient.

The maximum power dissipation can be calculated by following formula :

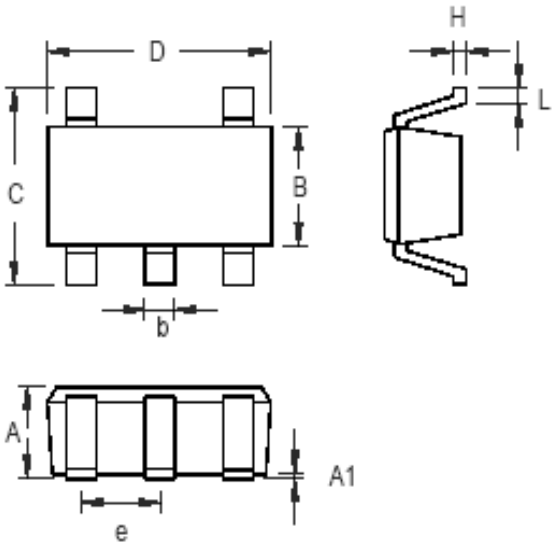
$$PD(MAX) = (TJ(MAX) - TA) / \theta JA$$

Where TJ(MAX) is the maximum operation junction temperature 125°C, TA is the ambient temperature and the θJA is the junction to ambient thermal resistance. For recommended operating conditions specification of LP3982, where TJ(MAX) is the maximum junction temperature of the die (125°C) and TA is the maximum ambient temperature. The junction to ambient thermal resistance (θJA is layout dependent) for SC-70-5 package is 250°C/W.

$$PD(MAX) = (125°C-25°C) / 250 = 400mW \text{ (SC-70-5)}$$

The maximum power dissipation depends on operating ambient temperature for fixed TJ(MAX) and thermal resistance θJA.

Packaging Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.100	0.031	0.044
A1	0.000	0.100	0.000	0.004
B	1.150	1.350	0.045	0.054
b	0.150	0.400	0.006	0.016
C	1.800	2.450	0.071	0.096
D	1.800	2.250	0.071	0.089
e	0.650		0.026	
H	0.080	0.260	0.003	0.010
L	0.210	0.460	0.008	0.018

SC-70-5 Surface Mount Package