300mA, Dual Channel Ultra-Fast CMOS LDO Regulato

General Description

The LP2201 is a dual channel, low noise, and low dropout regulator sourcing up to 300mA at each channel. The range of output voltage is from 1.2V to 3.6V from operating from 2.5V to 5.5V input.

LP2201 offers 2% accuracy, extremely low dropout voltage (80mV @ 100mA), and extremely low ground current, only 25μA per LDO. The shutdown current is near zero current which is suitable for battery-power devices. Other features include current limiting, over temperature, output short circuit protection.

LP2201 is short circuit thermal folded back protected. LP2201 lowers its OTP trip point from 165°C to 110°C when output short circuit occurs (VOUT<0.4V) providing maximum safety to end users.

LP2201 can operate stably with very small ceramic output capacitors, reducing required board space and component cost. LP2201 is available in fixed output voltages in the SOT-23-6 package.

Features

- Wide Operating Voltage Ranges : 2.5V to 5.5V
- Low-Noise for RF Application
- High PSRR 65dB at 1kHz
- No Noise Bypass Capacitor Required
- Fast Response in Line/Load Transient
- TTL-Logic-Controlled Shutdown Input
- Dual LDO Outputs (200mA/200mA)
- High Output Accuracy 2%
- Ultra-low Quiescent Current 27uA
- Thermal Shutdown Protection
- Tiny USP-6 Package
- RoHS Compliant and 100% Lead (Pb)-Free

Applications

- CDMA/GSM Cellular Handsets
- Smart mobile phone
- Battery-Powered Equipment
- DSC Sensor
- Wireless Card

Order Information

LP2203 □ □ □ □ □

F: Pb-Free

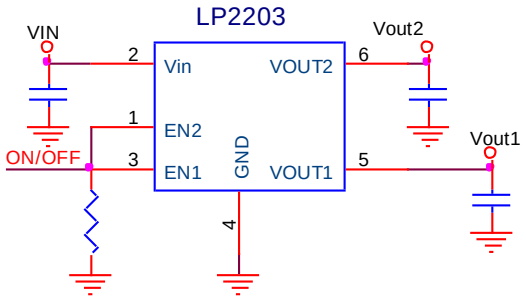
Package Type

U6: USP-6

Out1/Out2 Voltage Type

18/28: 1.8V/2.8V
18/33: 1.8V/3.3V
18/26: 1.8V/2.6V
25/28: 2.5V/2.8V
28/28: 2.8V/2.8V
28/12: 2.8V/1.2V
28/33: 2.8V/3.3V
30/30: 3.0V/3.0V
30/33: 3.0V/3.3V
33/33: 3.3V/3.3V

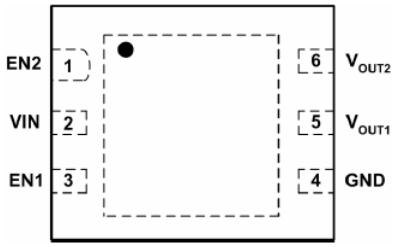
Typical Application Circuit



Marking Information

Device	Marking	Package	Shipping
LP2203		USP-6	3K/REEL

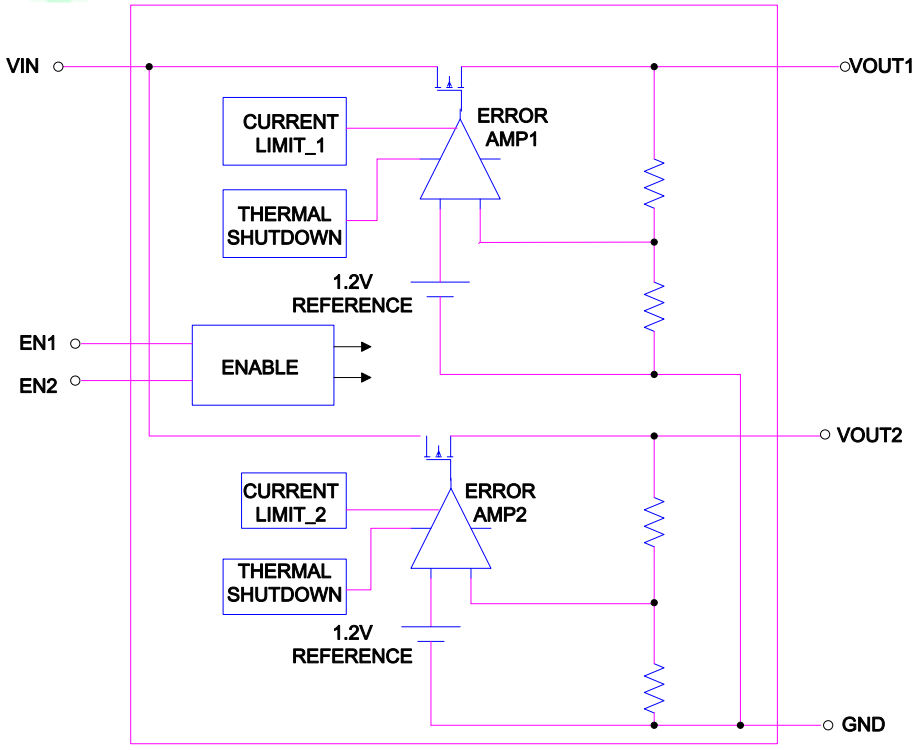
Functional Pin Description

Package Type	Pin Configurations
USP-6	

Pin Description

Pin	Name	Description
1	EN2	Chip Enable2 (Active High)
2	VIN	Supply Input
3	EN1	Chip Enable1 (Active High)
4	GND	Common Ground
5	VOUT1	Channel 1 Output Voltage
6	VOUT2	Channel2 Output Voltage

Function Diagram



Absolute Maximum Ratings

✧ Supply Input Voltage ---------- 6V

Power Dissipation, PD @ TA = 25°C

✧ USP-6 ---------- 450mW

Package Thermal Resistance

✧ USP-6, θJA ---------- 250°C/W

✧ Lead Temperature (Soldering, 10 sec.) ---------- 260°C

✧ Storage Temperature Range ---------- −65°C to 150°C

ESD Susceptibility

✧ HBM (Human Body Mode) ---------- 2kV

✧ MM(Machine-Mode) ---------- 200V

Recommended Operating Conditions

✧ Operation Junction Temperature Range ---------- −40°C to 125°C

✧ Operation Ambient Temperature Range ---------- −40°C to 85°C

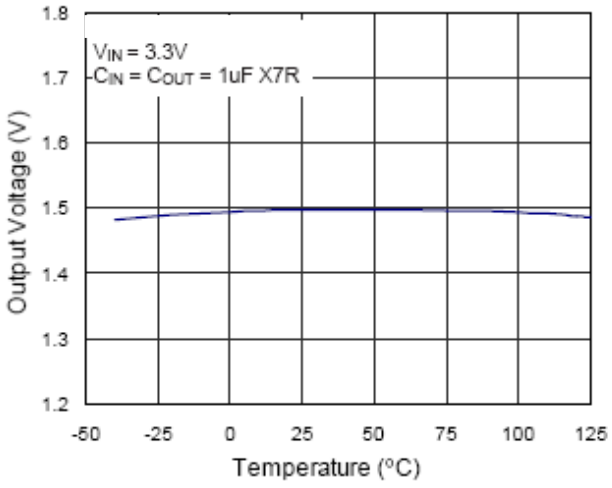
Electrical Characteristics

(VIN = VOUT + 1V, CIN = COUT = 1μF, TA = 25° C, unless otherwise specified)

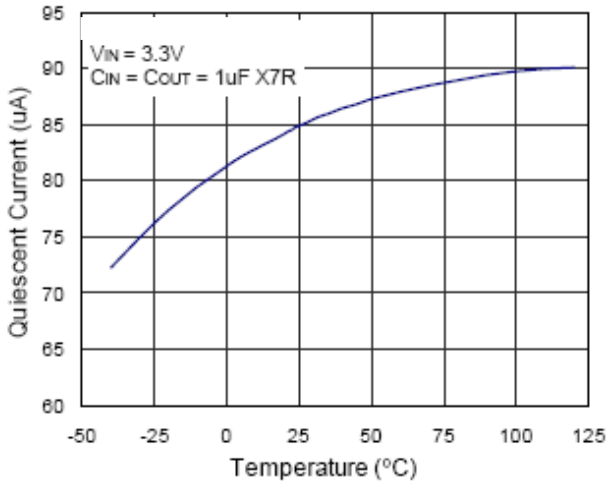
Parameter		Symbol	Test Conditions	Min	Typ	Max	Units
Output Voltage Accuracy		ΔVOUT	IOUT = 1mA	−2	--	+2	%
Maximum output Current		Imax	Continuous	200	250		mA
Current Limit		ILIM	RLOAD = 1Ω	360	400	700	mA
Quiescent Current		IQ	VEN ≥ 1.2V, IOUT = 0mA		75	110	μA
Dropout Voltage		VDROP	IOUT = 30mA, VOUT > 2.8V		30	45	mV
			IOUT = 150mA, VOUT > 2.8V		80	150	mV
Line Regulation		ΔVLINE	VIN = (VOUT + 1V) to 5.5V, IOUT = 1mA			0.3	%
Load Regulation		ΔLOAD	1mA < IOUT < 300mA			2	%
Standby Current		ISTBY	VEN = GND, Shutdown		0.01	1	μA
EN Input Bias Current		IIBSD	VEN = GND or VIN		1	5	uA
EN Threshold	Logic-Low Voltage	VIL	VIN = 3V to 5.5V, Shutdown			0.4	V
	Logic-High Voltage	VIH	VIN = 3V to 5.5V, Start-Up	1.2			V
Output Noise Voltage			10Hz to 100kHz, IOUT = 200mA COUT = 1μF		100		uVRMS
Power Supply	f = 100Hz	PSRR	COUT = 1μF, IOUT = 10mA	−75			dB
Rejection Rate	f = 10kHz			−65			dB
Thermal Shutdown Temperature		TSD			150		°C

Typical Operating Characteristics

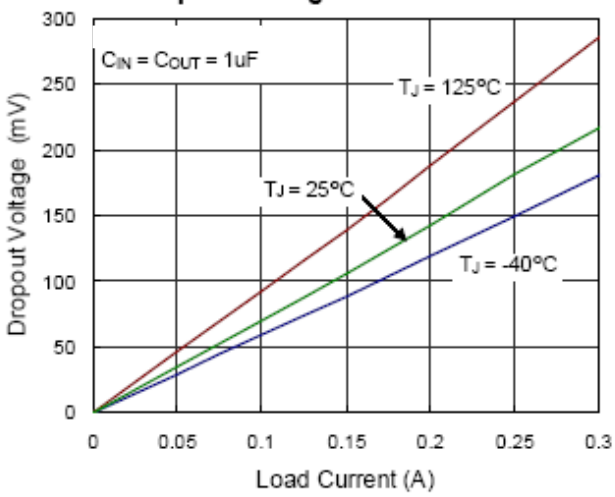
Output Voltage vs. Temperature



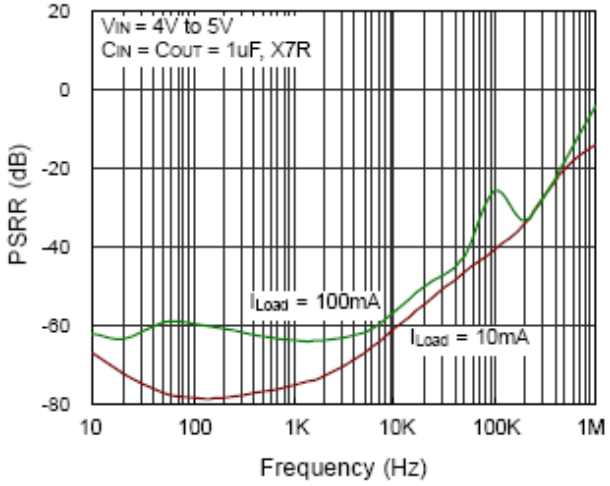
Quiescent Current vs. Temperature



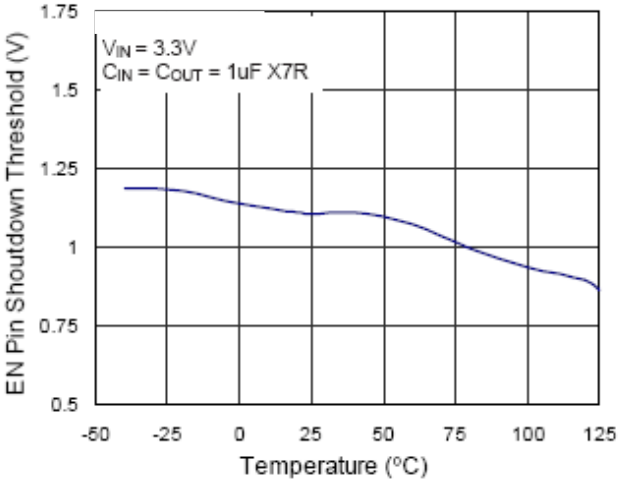
Dropout Voltage vs. Load Current



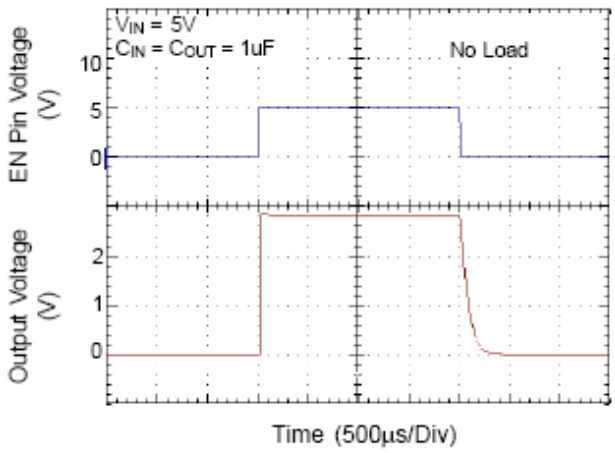
PSRR

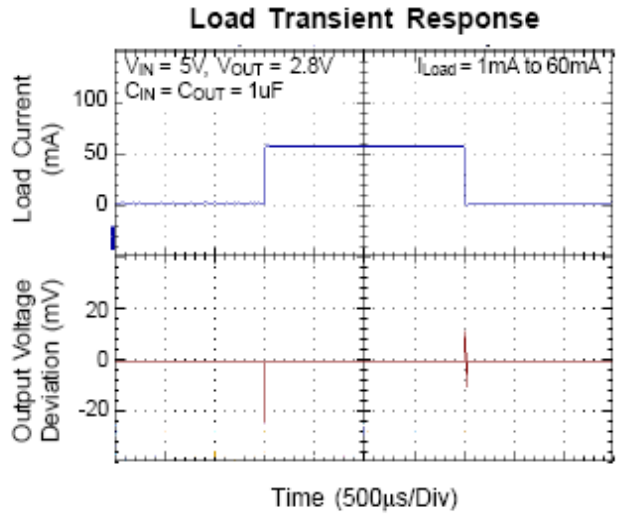


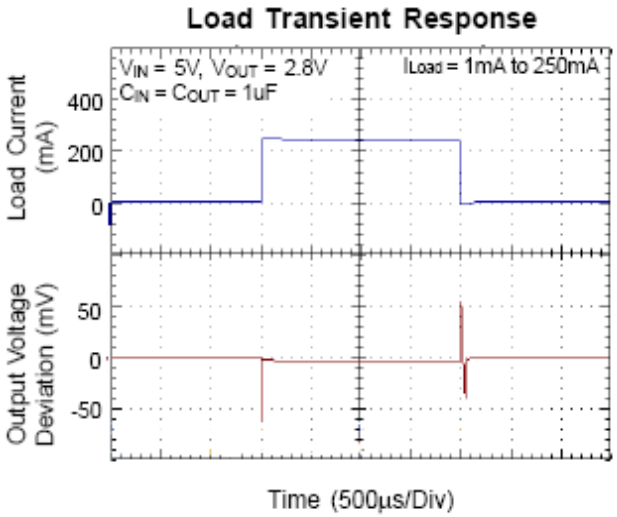
EN Pin Shoutdown Threshold vs. Temperature

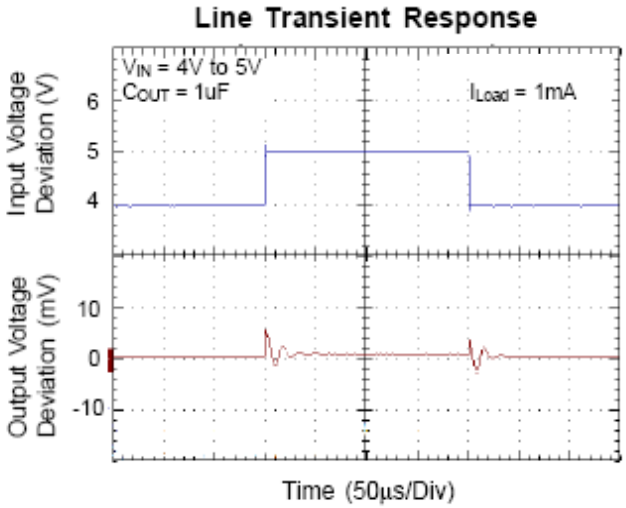


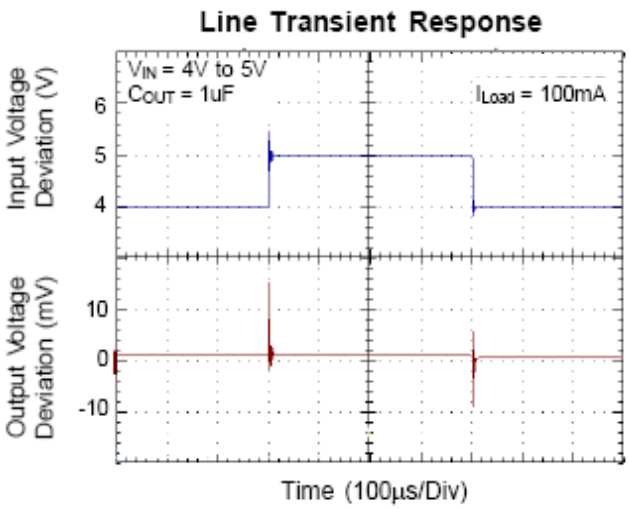
EN Pin Shutdown Response

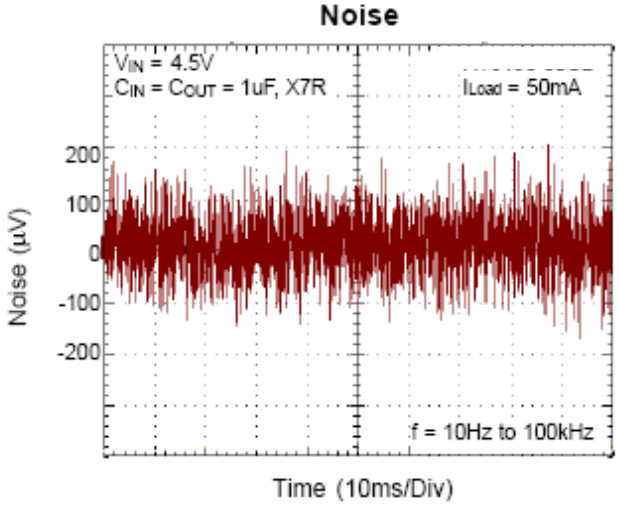


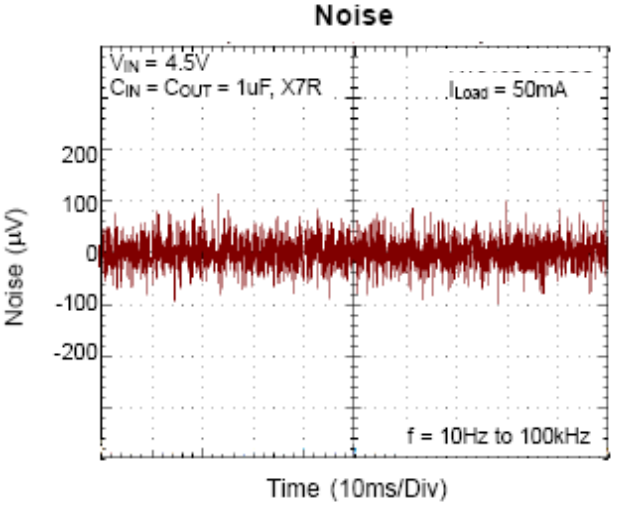

Load Transient Response
VIN = 5V, VOUT = 2.8V
CIN = COUT = 1uF
ILoad = 1mA to 60mA
Load Current (mA)
100
50
0
Output Voltage Deviation (mV)
20
0
-20
Time (500µs/Div)


Load Transient Response
VIN = 5V, VOUT = 2.8V
CIN = COUT = 1uF
ILoad = 1mA to 250mA
Load Current (mA)
400
200
0
Output Voltage Deviation (mV)
50
0
-50
Time (500µs/Div)


Line Transient Response
VIN = 4V to 5V
COUT = 1uF
ILoad = 1mA
Input Voltage Deviation (V)
6
5
4
Output Voltage Deviation (mV)
10
0
-10
Time (50µs/Div)


Line Transient Response
VIN = 4V to 5V
COUT = 1uF
ILoad = 100mA
Input Voltage Deviation (V)
6
5
4
Output Voltage Deviation (mV)
10
0
-10
Time (100µs/Div)


Noise
VIN = 4.5V
CIN = COUT = 1uF, X7R
ILoad = 50mA
Noise (µV)
200
100
0
-100
-200
f = 10Hz to 100kHz
Time (10ms/Div)


Noise
VIN = 4.5V
CIN = COUT = 1uF, X7R
ILoad = 50mA
Noise (µV)
200
100
0
-100
-200
f = 10Hz to 100kHz
Time (10ms/Div)

Applications Information

Like any low-dropout regulator, the external capacitors used with the LP2203 must be carefully selected for regulator stability and performance. Using a capacitor whose value is > 1μF on the LP2203 input and the amount of capacitance can be increased without limitation. The input capacitor must be located a distance of not more than 0.5 inch from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response. The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDO application. The LP2203 is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least 1μF with ESR is > 25mΩ on the LP2203 output ensures stability. The LP2203 still works well with output capacitor of other types due to the wide stable ESR range. Figure 1 shows the curves of allowable ESR range as a function of load current for various output capacitor values. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located not more than 0.5 inch from the VOUT pin of the LP2203 and returned to a clean analog ground.

Start-up Function Enable Function

The LP2203 features an LDO regulator enable/disable function. To ensure the LDO regulator will switch on, the EN turn on control level must be greater than 1.2 volts. The LDO regulator will go into the shutdown mode when the voltage on the EN pin falls below 0.4 volts. To protect the system, the LP2203 have a quick-discharge function. If the enable function is not needed in a specific application, it may be tied to VIN to keep the LDO regulator in a continuously on- state mode.

Thermal Considerations

Thermal protection limits power dissipation in LP2201. When the operation junction temperature exceeds 150°C, the OTP circuit starts the thermal shutdown function turn the pass element off. The pass element turn on again after the junction temperature cools by 25°C. For continuous operation, do not exceed absolute maximum operation junction temperature 125°C.

The power dissipation definition in device is :

$$PD = (VIN-VOUT) \times IOUT + VIN \times IQ$$

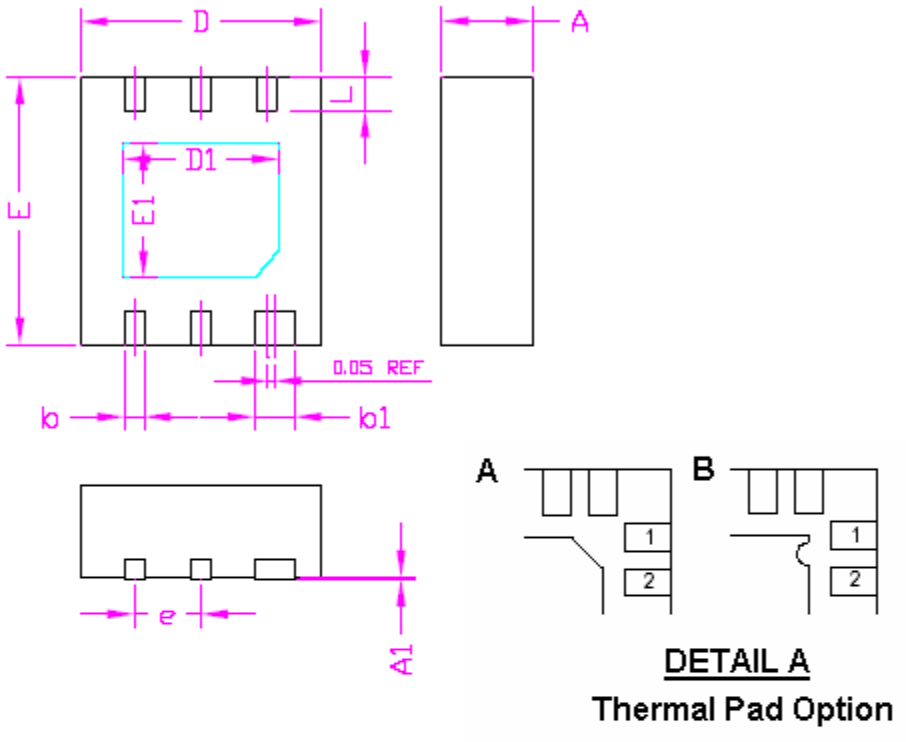
The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient.

The maximum power dissipation can be calculated by following formula :

$$PD(MAX) = (TJ(MAX) - TA) / \theta JA$$

Package Information

USP-6



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
b	0.10	0.30	0.004	0.012
b1	0.20	0.40	0.008	0.016
D	1.70	1.90	0.067	0.075
D1	1.50		0.059	
E	1.90	2.10	0.075	0.083
E1	0.90		0.035	
e	0.50		0.020	
L	0.15	0.35	0.006	0.014