Full Bridge Gate Driver with Boost Convertor

General Description

LP1115 consists of two parts: Full Bridge Gate Drive and Boost Convertor.

The Full Bridge Driver part of LP1115 is a single phase 12V MOSFET gate driver optimized to drive the gates of both high-side and low-side power MOSFETs in a synchronous buck converter.

The Boost Convertor part of LP1115 is a current mode boost DC-DC converter. Its PWM circuitry with built-in 3A current power MOSFET makes this converter highly power efficiently. The LP1115 implements a constant frequency 1MHz PWM control scheme. The high frequency PWM operation also saves board space by reducing external component sizes.

Features

- Full Bridge Driver
  - All-In-One Synchronous Buck Driver
  - Bootstrapped High-Side Drive
  - One PWM Signal Generates Both Drives
  - Anti-cross Conduction Protection Circuitry
- Boost Convertor
  - Up to 94% efficiency
  - Shut-down current:1uA
  - Input and Output voltage Up to 24V
  - Internal Compensation, Soft-start
  - 1MHz fixed frequency switching
  - High switch on current:3A

Order Information

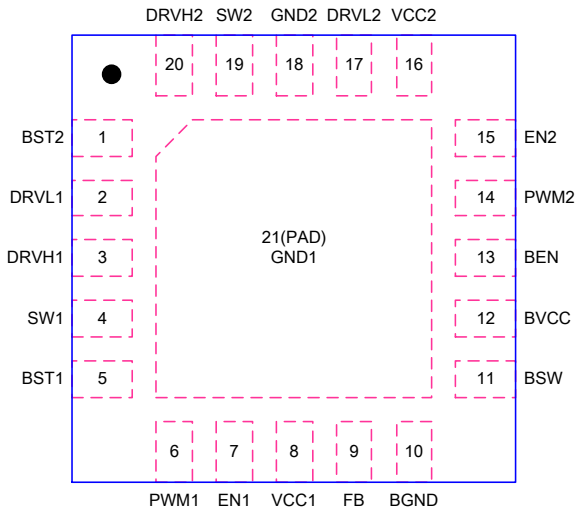
LP1115 □□ □□ □

- F: Pb-Free
- Package Type
  - QV: QFN-20
- Feedback Voltage
  - Default: 0.6V
  - A: 1.24V

Marking Information

Device	Marking	Package	Shipping
LP1115QVF	LPS LP1115 YWX	QFN-20 (4mm*4mm)	3K/REEL
LP1115AQVF	LPS LP1115A YWX	QFN-20 (4mm*4mm)	3K/REEL
Marking indication: Y:Production year W:Production week X: Series Number			

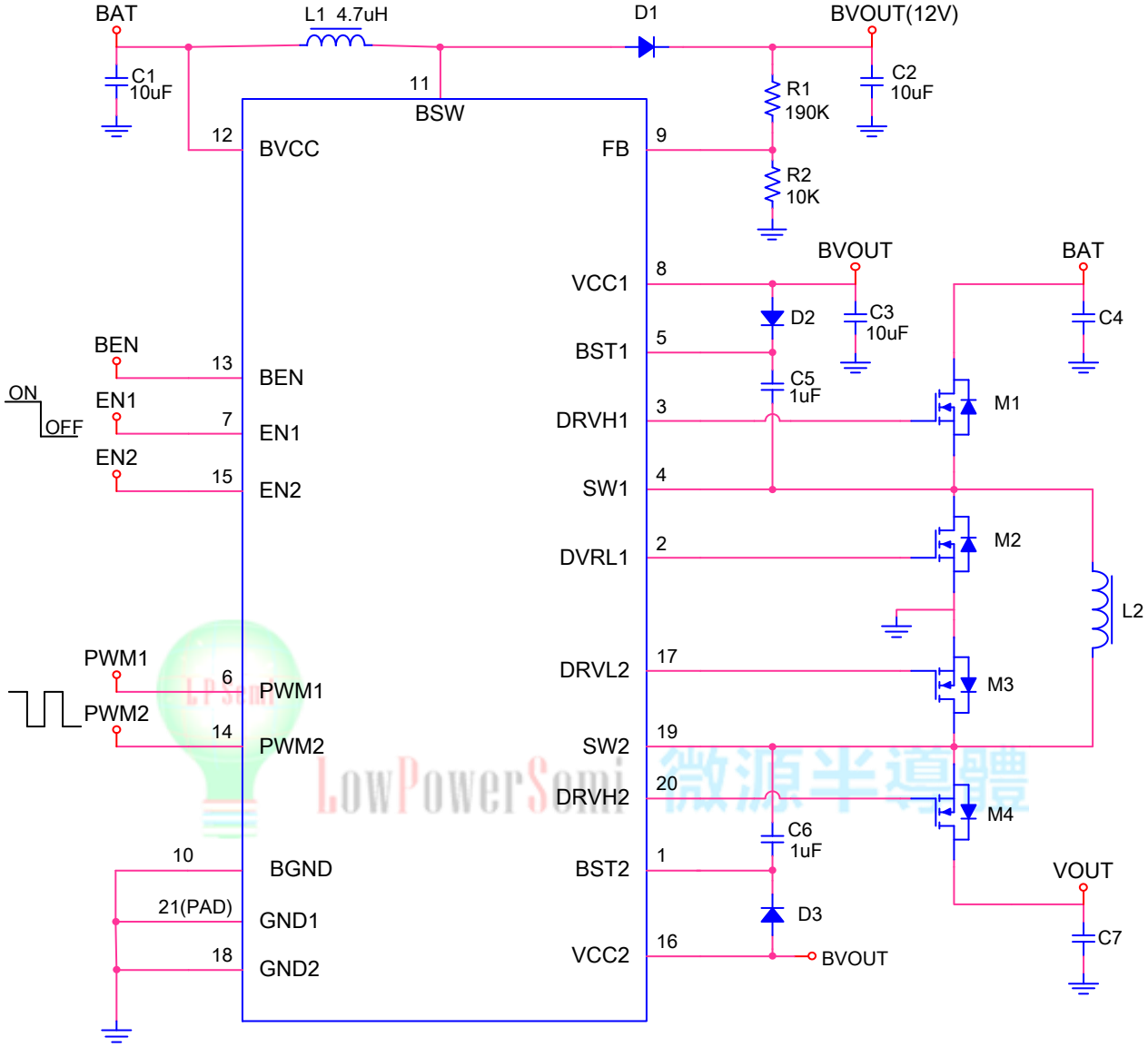
Functional Pin Description

Package Type	Pin Configurations
QFN-20 (Top View)	

Pin Description

Pin No.	Name	Description
1	BST2	Channel 2. Upper MOSFET Floating Bootstrap Supply.
2	DRVL1	Channel 1. Output Drive for the lower MOSFET.
3	DRVH1	Channel 1. Output Drive for the upper MOSFET.
4	SW1	Channel 1. Switch Node. Connect to the source of the upper MOSFET.
5	BST1	Channel 1. Upper MOSFET Floating Bootstrap Supply.
6	PWM1	Channel 1. Logic-Level Input. This pin has primary control of the drive outputs.
7	EN1	Channel 1. Output Disable. When low, normal operation is disabled forcing DRVH1 and DRVL1 low.
8	VCC1	Channel 1. Input Supply. A 1μF ceramic capacitor should be connected from this pin to GND1.
9	FB	Boost. Regulation Feedback Input.
10	BGND	Boost. Ground.
11	BSW	Boost. Switch Node.
12	BVCC	Boost. Power Supply pin.
13	BEN	Boost. Output Disable. When low, boost enter low current shutdown mode.
14	PWM2	Channel 2. Logic-Level Input. This pin has primary control of the drive outputs.
15	EN2	Channel 2. Output Disable. When low, normal operation is disabled forcing DRVH2 and DRVL2 low.
16	VCC2	Channel 2. Input Supply. A 1μF ceramic capacitor should be connected from this pin to GND2.
17	DRVL2	Channel 2. Output Drive for the lower MOSFET.
18	GND2	Channel 2. Power Ground. Should be closely connected to the source of the lower MOSFET.
19	SW2	Channel 2. Switch Node. Connect to the source of the upper MOSFET.
20	DRVH2	Channel 2. Output Drive for the upper MOSFET.
21(PAD)	GND1	Channel 1. Power Ground. Should be closely connected to the source of the lower MOSFET.

Typical Application Circuit



Absolute Maximum Ratings Note 1

- ✧ VCC1/2 to GND1/2 ---------- -0.3V to 15V
- ✧ EN1/2 to GND1/2 ---------- -0.3V to 15V
- ✧ BST1/2 to GND1/2 ---------- -0.3V to 35V
- ✧ BST1/2 to SW1/2 ---------- -0.3V to 15V
- ✧ SW1/2 to GND1/2---------- -5V to 20V
- ✧ DRVH1/2 to GND1/2 ---------- SW1/2-0.3V to BST1/2+0.3V
- ✧ DRVL1/2 to GND1/2 ---------- -0.3V to VCC1/2+0.3V
- ✧ PWM1/2 to GND1/2 ---------- -0.3V to 6.5V
- ✧ BVCC to BGND ---------- -0.3V to 26V
- ✧ BSW to BGND ---------- -0.3V to 30V
- ✧ BEN to BGND ---------- -0.3V to 26V
- ✧ FB to BGND ---------- -0.3V to 6V
- ✧ Maximum Junction Temperature ---------- 150℃
- ✧ Maximum Soldering Temperature (at leads,10 sec) ---------- 260℃
- ✧ Storage Temperature ---------- -65℃ to 150℃
- ✧ Operating Ambient Temperature Range ---------- -40℃ to 85℃

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Information

- ✧ Maximum Power Dissipation (P_D, T_A=25℃) ---------- 2.5W
- ✧ Thermal Resistance (θ_{JA}) ---------- 50℃/W

ESD Susceptibility

- ✧ HBM(Human Body Mode) ---------- 2KV
- ✧ MM(Machine Mode) ---------- 200V

Electrical Characteristics

(T_A=25℃, V_{IN} = 5V, unless otherwise noted.)

Full Bridge Driver

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage Range	V_{CC}	–	4.3	–	13.2	V
Supply Current	I_{SYS}	V_{BST} = 12V, V_{IN} = 0V, V_{EN}=0V	–	0.7	–	mA
EN Input Voltage High	V_{EN_HI}	–	2.0	–	–	V
EN Input Voltage Low	V_{EN_LO}	–	–	–	0.8	V
EN Hysteresis		–	–	300	–	mV
EN Input Current		No internal pull-up or pull-down resistors	−1.0	–	+1.0	μA
PWM Input Voltage High	V_{PWM_HI}	–	2.0	–	–	V
PWM Input Voltage Low	V_{PWM_LO}	–	–	–	0.8	V
PWM Hysteresis	–	–	–	300	–	mV
PWM Input Current	–	No internal pull-up or pull-down resistors	−1.0	–	+1.0	μA
High-Side Driver						
Output Resistance, Sourcing Current	–	V_{BST} – V_{SW} = 12 V	–	3.3	-	Ω
Output Resistance, Sinking Current	–	V_{BST} – V_{SW} = 12 V	–	0.5	-	Ω
Output Resistance, Unbiased	–	V_{BST} – VSW = 0 V	–	15	-	kΩ
Transition Times	T_{rDRVH}	V_{BST} – V_{SW} = 12 V, C_{LOAD} = 3.0 nF (See Figure 2)	–	30	-	ns
	T_{fDRVH}			12	-	ns
Propagation Delay Times	$T_{pdhDRVH}$	V_{BST} – V_{SW} = 12 V, C_{LOAD} = 3.0 nF (See Figure 2)	-	95	-	ns
	$T_{pdlDRVH}$	V_{BST} – V_{SW} = 12 V, C_{LOAD} = 3.0 nF (See Figure 2)		15	-	ns
	T_{pdlEN}	(See Figure 1)		30	-	ns
	T_{pdhEN}	(See Figure 1)		35	-	ns
SW Pull down Resistance	–	V_{SW} = GND	–	15	–	kΩ
Low-Side Driver						
Output Resistance, Sourcing Current	–		–	3.3	-	Ω
Output Resistance, Sinking Current	–		–	0.5	–	Ω
Output Resistance, Unbiased	–	V_{CC} = GND	–	15	–	kΩ
Transition Times	T_{rDRVL}	C_{LOAD} = 3.0 nF, (See Figure 2)	–	30	-	ns
	T_{fDRVL}			12	-	ns
Propagation Delay Times	$T_{pdhDRVL}$	C_{LOAD} = 3.0 nF, (See Figure 2)	–	105	-	ns
	$T_{pdlDRVL}$		-	15	-	ns
	T_{pdlEN}	(See Figure 1)	-	30	-	ns
	T_{pdhEN}	(See Figure 1)	-	35	-	ns
Timeout Delay	–	V_{DRVH} – V_{SW} = 0	–	110	–	ns
UVLO Startup	–	–	-	4.2	-	V
UVLO Shutdown	–	–	-	3.8	-	V
UVLO Hysteresis	–	–	-	0.3	-	V

Boost Convertor

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		2.5		24	V
Output Voltage Range	-		2.5		24	V
Supply Current(Shutdown)	-	V_{EN} = 0V, V_{SW} = 5V		1		μA
Supply Current	I_{SYS}	V_{FB} = 0.7V		3.5		mA
Feedback Voltage	V_{FB}	LP1115QVF	0.588	0.6	0.612	V
		LP1115AQVF	1.215	1.24	1.265	V
Feedback Input Current	I_{FB}	V_{FB} = 1.2V		50		nA
Switching Frequency	f_{OSC}			1		MHz
Maximum Duty Cycle	-		85	92	98	%
EN Input Low Voltage	V_{EN_L}				0.4	V
EN Input High Voltage	V_{EN_H}		1.4			V
EN input current	I_{EN}	V_{EN} = 5		1		μA
Switch MOSFET Current Limit	-			3		A
High-side On Resistance	$R_{DS(ON)}$	V_{OUT} = 5V		150		mΩ

Timing Diagram

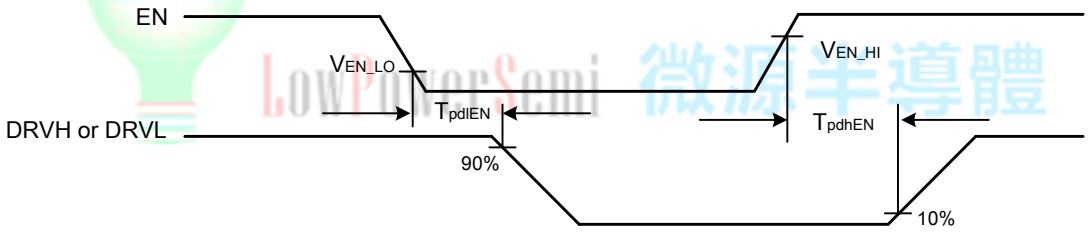


Figure1.EN Timing waveforms

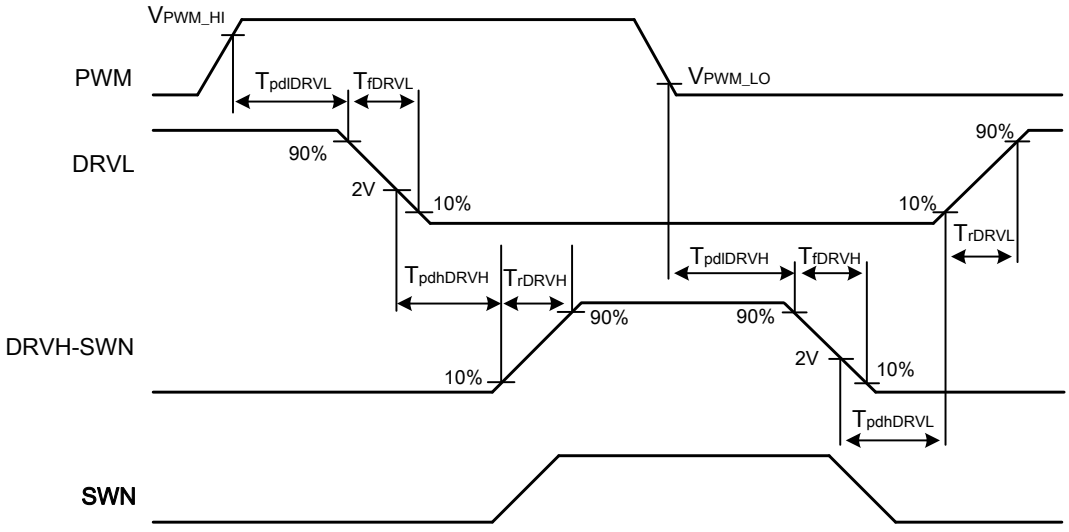


Figure2.Input-Output Timing waveforms

Operation Information (Full Bridge Driver)

The Full Bridge Driver part of LP1115 is a single phase MOSFET driver for driving two N-channel MOSFETs in a synchronous buck converter topology. The LP1115 will operate from 5V or 12V, but have been optimized for high current multi-phase buck regulators that convert 12V rail directly to the core voltage required by complex logic chips.

A single PWM input signal is all that is required to properly drive the high-side and the low-side MOSFETs. Each driver is capable of driving a 3nF load at frequencies up to 1 MHz.

High-Side Driver

The high−side driver is designed to drive a floating low $R_{DS(ON)}$ N-channel MOSFET. The gate voltage for the high side driver is developed by a bootstrap circuit referenced to Switch Node (SW) pin.

The bootstrap circuit is comprised of an external diode, and an external bootstrap capacitor. When the LP1115 are starting up, the SW pin is at ground, so the bootstrap capacitor will charge up to VCC through the bootstrap diode. When the PWM input goes high, the high-side driver will begin to turn on the high-side MOSFET using the stored charge of the bootstrap capacitor. As the high-side MOSFET turns on, the SW pin will rise. When the high-side

MOSFET is fully on, the switch node will be at 12V, and the BST pin will be at 12V plus the charge of the bootstrap capacitor (approaching 24V).The bootstrap capacitor is recharged when the switch node goes low during the next cycle.

Low-Side Driver

The low-side driver is designed to drive a ground-referenced low $R_{DS(ON)}$ N-Channel MOSFET. The voltage rail for the low-side driver is internally connected to the VCC supply and GND.

Safety Timer and Overlap Protection Circuit

It is very important that MOSFETs in a synchronous buck regulator do not both conduct at the same time. Excessive shoot-through or cross conduction can damage the MOSFETs, and even a small amount of cross conduction will cause a decrease in the power conversion efficiency.

The LP1115 prevent cross conduction by monitoring the status of the external MOSFETs and applying the appropriate amount of “dead-time” or the time between the turn off of one MOSFET and the turn on of the other MOSFET. When the PWM input pin goes high, DRVL will go low after a propagation delay ($T_{pdlDRVL}$). The time it takes for the low-side MOSFET to turn off (T_{fDRVL}) is dependent on the total charge on the low-side MOSFET gate. The LP1115 monitor the gate voltage of both MOSFETs and the switch node voltage to determine the conduction status of the MOSFETs. Once the low−side MOSFET is turned off an internal timer will delay ($T_{pdhDRVH}$) the turn on of the high-side MOSFET.

Likewise, when the PWM input pin goes low, DRVH will go low after the propagation delay ($T_{pdlDRVH}$). The time to turn off the high-side MOSFET (T_{fDRVH}) is dependent on the total gate charge of the high−side MOSFET. A timer will be triggered once the high-side MOSFET has stopped conducting, to delay ($T_{pdhDRVL}$) the turn on of the low-side MOSFET.

Power Supply Decoupling

The LP1115 can source and sink relatively large currents to the gate pins of the external MOSFETs. In order to maintain a constant and stable supply voltage (VCC) a low ESR capacitor should be placed near the power and ground pins. A 1μF to 4.7μF multilayer ceramic capacitor is usually sufficient.

Input Pins

The PWM pin of the LP1115 has internal protection for Electro Static Discharge (ESD), but in normal operation they present relatively high input impedance. If the PWM controller does not have internal pull-down resistors, they should be added externally to ensure that the driver outputs do not go high before the controller has reached its under voltage lockout threshold.

Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor (C_{BST}) and the external diode. Selection of these components can be done after the high-side MOSFET has been chosen. The bootstrap capacitor must have a voltage rating that is able to withstand twice the maximum supply voltage. A minimum 50V rating is recommended. The capacitance is determined using the following equation:

$$C_{BST} = \frac{Q_{GATE}}{\Delta V_{BST}}$$

Where Q_{GATE} is the total gate charge of the high-side MOSFET, and ΔV_{BST} is the voltage droop allowed on the high-side MOSFET drive.

For example, an external MOSFET has a total gate charge of about 30nC. For an allowed droop of 300mV, the required bootstrap capacitance is 100nF. A good quality ceramic capacitor should be used. The bootstrap diode must be rated to withstand the maximum supply voltage plus any peak ringing voltages that may be present on SW. The average forward current can be estimated by:

$$I_{F(AVG)} = Q_{GATE} \times f_{MAX}$$

Where f_{MAX} is the maximum switching frequency of the controller. The peak surge current rating should be checked in-circuit, since this is dependent on the source impedance of the 12V supply and the ESR of C_{BST}.

Operation Information (Boost Convertor)

The Boost Convertor part of LP1115 uses a fixed frequency, peak current mode boost regulator architecture to regulate voltage at the feedback pin. At the start of each oscillator cycle the MOSFET is turned on through the control circuitry. To prevent sub-harmonic oscillations at duty cycles greater than 50 percent, a stabilizing ramp is added to the output of the current sense amplifier and the result is fed into the negative input of the PWM comparator. When this voltage equals the output voltage of the error amplifier the power MOSFET is turned off. The voltage at the output of the error amplifier is an amplified version of the difference between the 0.6V band gap reference voltage and the feedback voltage. In this way the peak current level keeps the output in regulation. If the feedback voltage starts to drop, the output of the error amplifier increases. These results in more current to flow through the power MOSFET, thus increasing the power delivered to the output.

The Boost Convertor part of LP1115 has internal soft start to limit the amount of input current at startup and to also limit the amount of overshoot on the output.

Setting the Output Voltage

Set the output voltage by selecting the resistive voltage divider ratio. The voltage divider drops the output voltage to the 0.6V feedback voltage. Use a 100K resistor for R_2 of the voltage divider. Determine the high-side resistor R_1 by the equation:

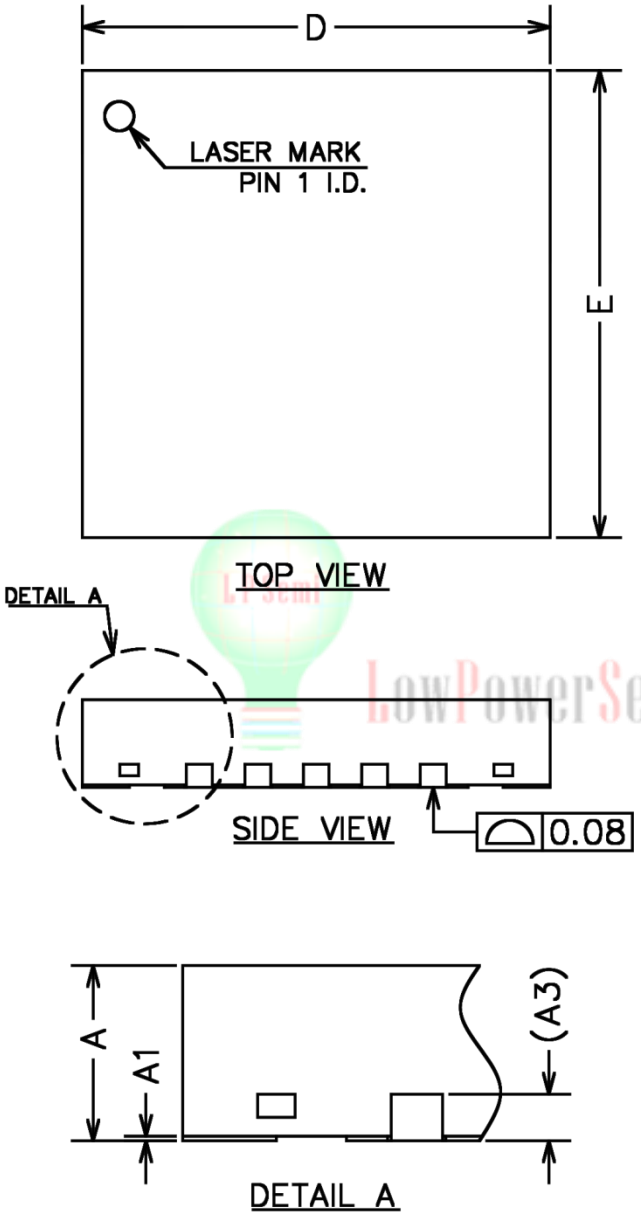
$$V_{OUT} = (R_1 / R_2 + 1) \times V_{FB}$$

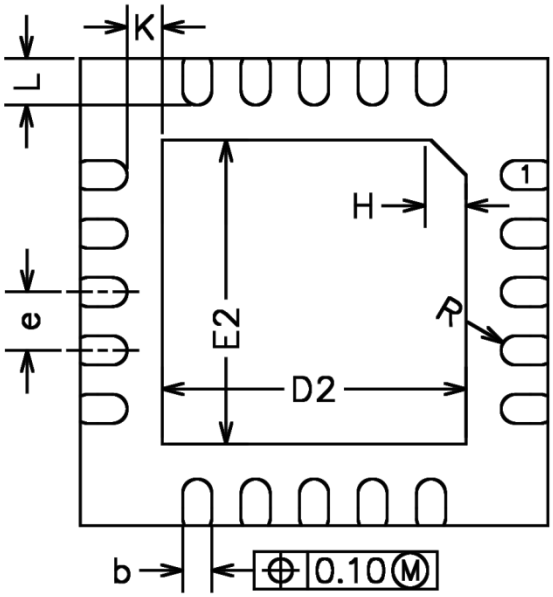
Current Limitation

The internal power-MOS switch current is monitored cycle-by-cycle and is limited to the value not exceed 3A(Typ.). When the switch current reaches the limited value, the internal power-MOS is turned off immediately until the next cycle. Keep traces at this pin as short as possible. Do not put capacitance at this pin.

Packaging Information

QFN-20





BOTTOM VIEW

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20REF	
b	0.20	0.25	0.30
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.50	2.60	2.70
E2	2.50	2.60	2.70
e	0.40	0.50	0.60
H		0.30REF	
K	0.20	–	–
L	0.35	0.40	0.45
R	0.10	–	–