Dual Channel Charge Pump Power Solution For TFT LCD Panel

General Description

The LP3102 DC/DC converter integrates two low noise, high efficiency charge pumps for dual outputs, which consist of one inverting output and a step-up output. The device operates from 2.5V to 4.8V input, and provides a step-up output voltage (VP) of 2x the input voltage. The negative inverting output (VN) is -1x inverted from the positive output VP.

The LP3102 is available in a small TDFN-10 pin package that features a bottom side exposed thermal pad to provide optimal heat dissipation. The small package size and low external parts count make the device ideally suitable for TFT LCD applications of mobile products. The device is rated to operate from -40℃ to +85℃ ambient temperature range.

Order Information

LP3102 □ □ □ □

- F: Pb-Free
- Package Type
  - QV: TDFN-10
- Output Type
  - Default: 5.5V ~ 5.9V

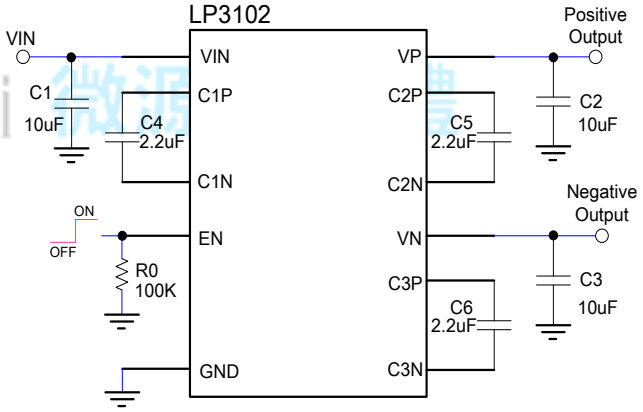
Applications

- ✧ Mobile Device, Smart Phone
- ✧ Portable Media Players/MP3 players
- ✧ Cellular and Smart mobile phone
- ✧ LCD Bias Power

Features

- ◆ Ultra-Low-Noise for RF Application
- ◆ 2.5V to 4.8V Input Supply Voltage Range
- ◆ Adaptive 1.5x / 2x mode switchover for positive voltage and -1x mode for negative voltage
- ◆ VP output range (V_{OUT} ≦ 2x V_{IN}):
  5.5V to 5.9V (LP3102QVF)
- ◆ VN output range (V_{OUT} ≦ 2x V_{IN}):
  -5.5V to -5.9V (LP3102QVF)
- ◆ High current output: Vin=3.3V, I_{OUT}=±120mA;
- ◆ Built in Power On Sequence
- ◆ TDFN-10 (3.0mm × 3.0mm) Package

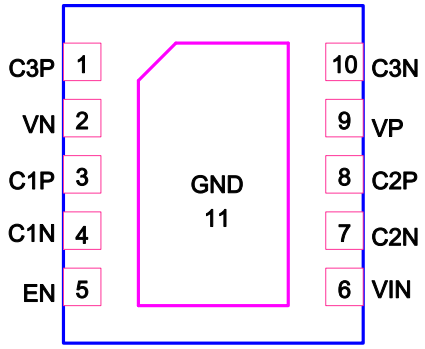
Typical Application Circuit



Marking Information

Device	Marking	Package	Shipping
LP3102QVF	LPS LP3102QVF YWX	TDFN-10	4K/REEL
Marking indication: Y:Production year W:Production week X:Production batch			

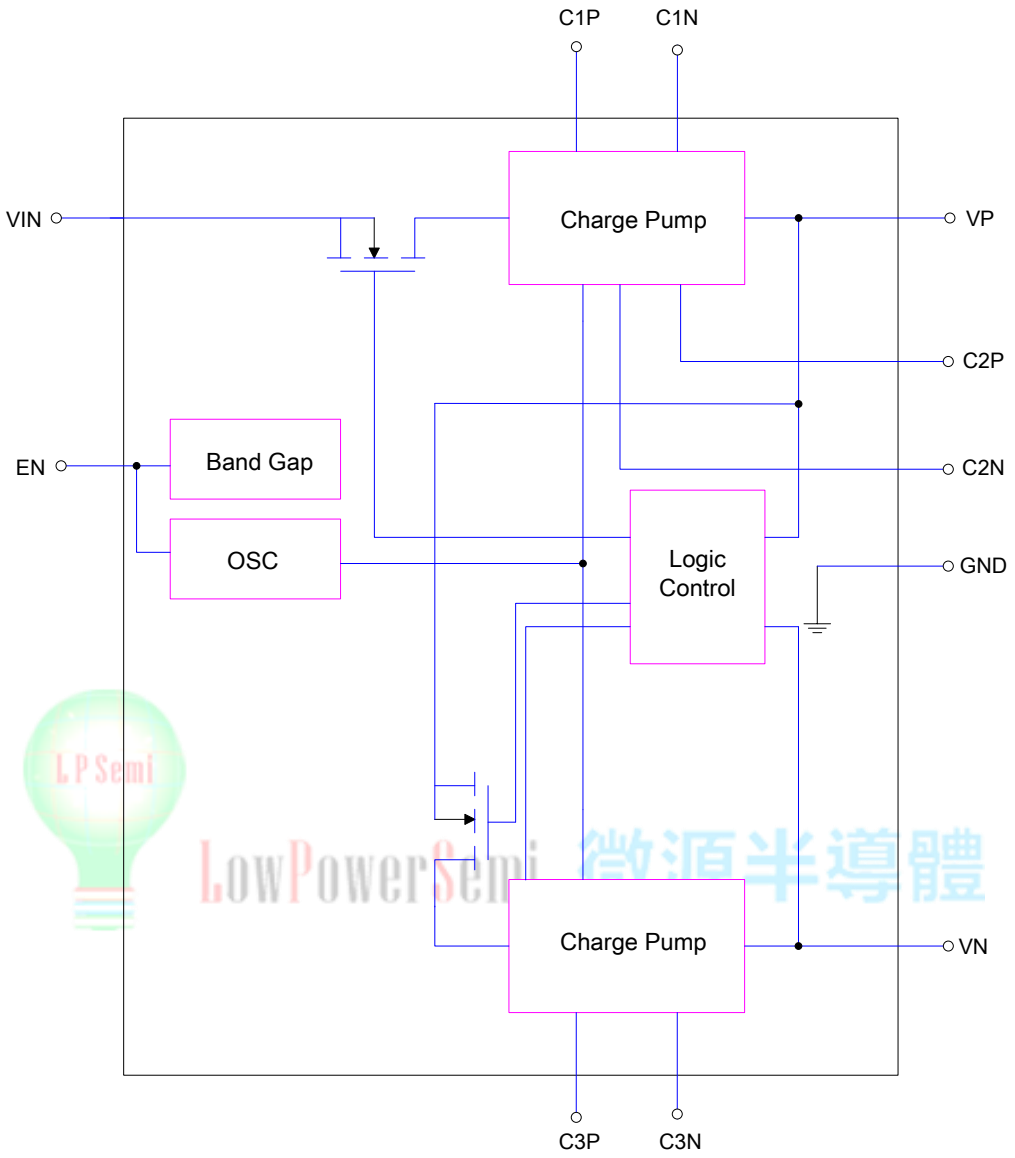
Functional Pin Description

Package Type	Pin Configurations
TDFN-10	

Pin Description

Pin	Name	Description
1	C3P	Flying Capacitor 1 Positive Terminal (C_6).
2	VN	Negative Output pin.
3	C1P	Flying Capacitor 1 Positive Terminal (C_4).
4	C1N	Flying Capacitor 1 Negative Terminal (C_4).
5	EN	Device Enable pin.
6	VIN	Input Supply Voltage. Bypass VIN with a low ESR ceramic capacitor to GND.
7	C2N	Flying Capacitor 1 Negative Terminal (C_5).
8	C2P	Flying Capacitor 1 Positive Terminal (C_5).
9	VP	Positive Output pin.
10	C3N	Flying Capacitor 1 Negative Terminal (C_6).
11(Pad)	GND	Ground pin.

Function Diagram



Absolute Maximum Ratings

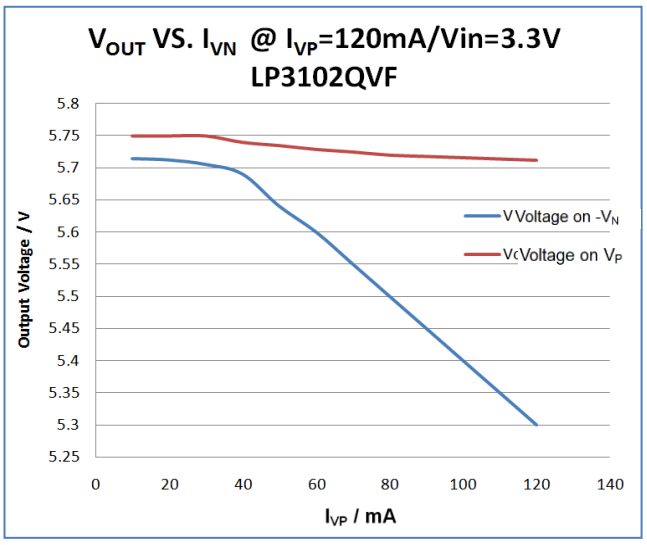
- ✧ Input / Output Voltage to GND ---------- -0.3V to 6V
- ✧ EN to GND ---------- -0.3V to VIN
- ✧ Maximum Junction Temperature ---------- 150℃
- ✧ Maximum Soldering Temperature (at leads, 10sec) ---------- 260℃
- ✧ Storage Temperature Range ---------- −65℃ to 165℃
- ✧ Operation Ambient Temperature Range ---------- -40℃ to 85℃
- ✧ Maximum Power Dissipation (PD, TA<40℃) ---------- 1.5W
- ✧ Thermal Resistance (J_A) ---------- 68℃/W

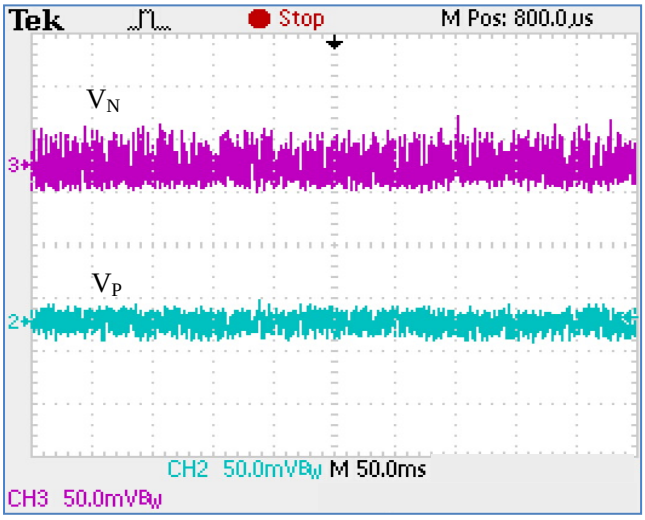
Electrical Characteristics

(V_{IN}=V_{EN}, C_1=C_2=C_3=2.2uF, C_4=C_5 =C_6=1uF, Typical values are T_A=25℃)

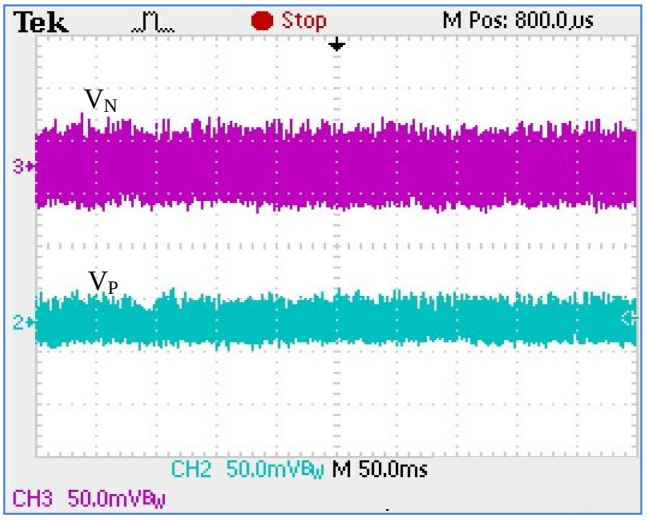
Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Input Voltage	V_{IN}		2.5		4.8	V
Output Current	I_{OUT}	Positive Output Current		120		mA
		Negative Output Current		120		
Positive Output Voltage	V_P	LP3102QVF	5.5		5.9	V
Negative Output Voltage	V_N	LP3102QVF	-5.9		-5.5	
Shutdown Current	I_{SHDN}	V_{EN}=GND, V_{IN}=3.6V			1	μA
Oscillator Frequency	f_{OSC}	I_{VP}=I_{VN}=10mA		300		KHz
EN Logic Low	V_{LL}				0.4	V
EN Logic High	V_{LH}		1.4			V
EN Pin Current	I_{EN}				0.5	μA
Thermal Shutdown Temperature	T_{SD}			145		℃

Typical Operating Characteristics

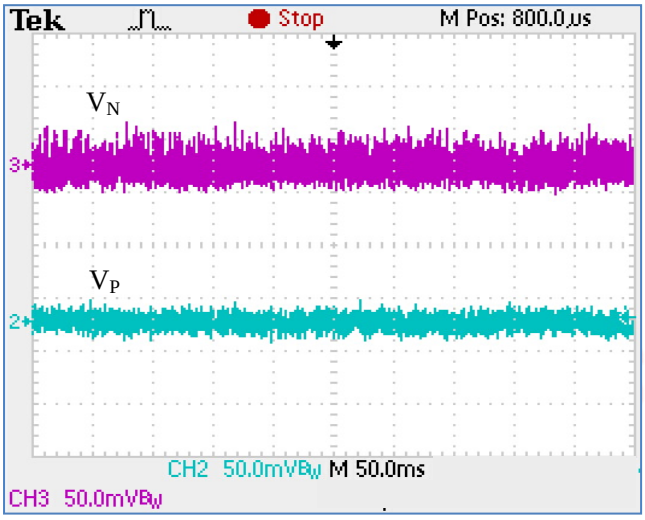




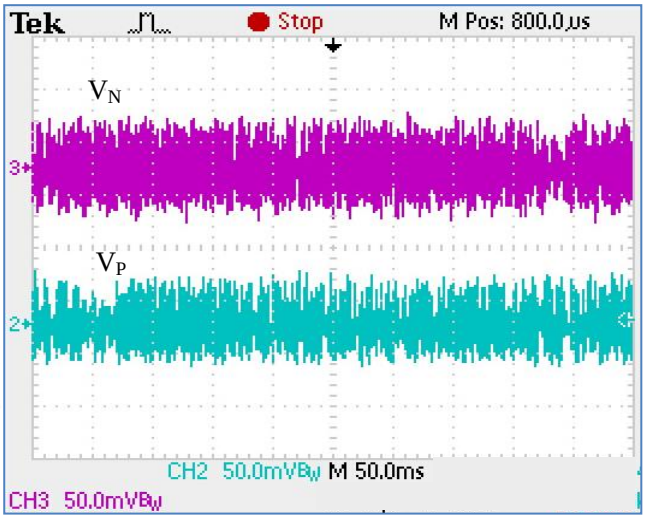
V_{IN}=3.3V, C_{OUT}=4.7uF, I_{VP}=I_{VN}=10mA



V_{IN}=3.3V, C_{OUT}=4.7uF, I_{VP}=I_{VN} =100mA



V_{IN}=3.3V, C_{OUT}=10uF, I_{VP}=I_{VN} =10mA



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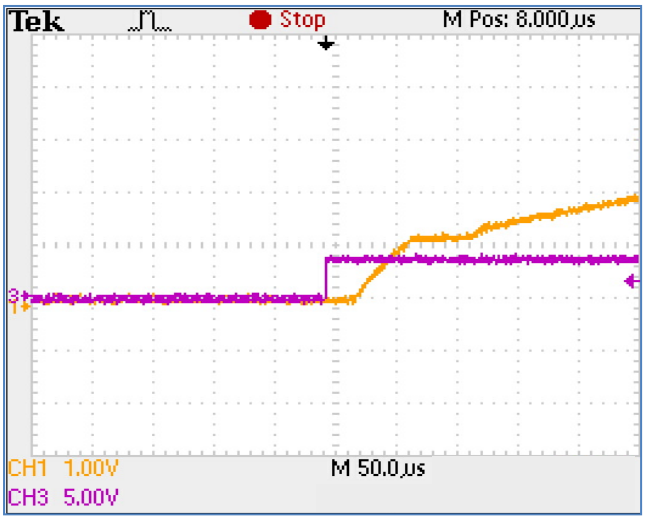
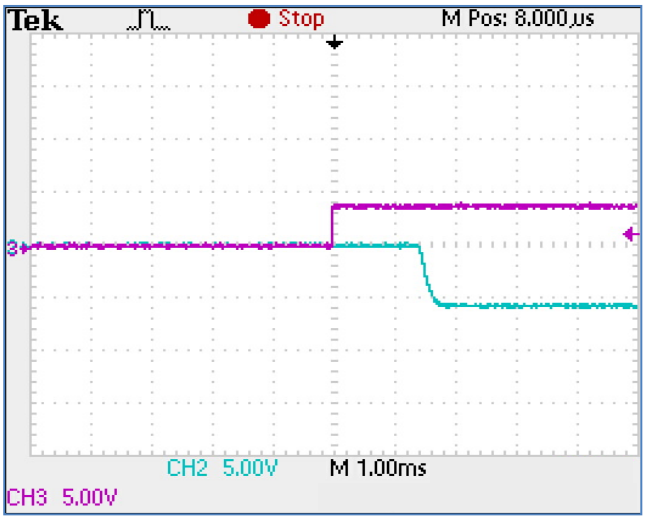


Start up Waveform with VP



Start up Waveform with VN

Application Information

The LP3102 offers dual channel output voltage for powering on specified power in TFT LCD panels. The device integrates a positive charge pump and a negative charge pump.

Enable Control (EN) to turn on the LP3102, the EN pin must be at logic high. When the EN pin is pulled to a logic low, the device is disabled and the supply current reduces to less than 1μA.

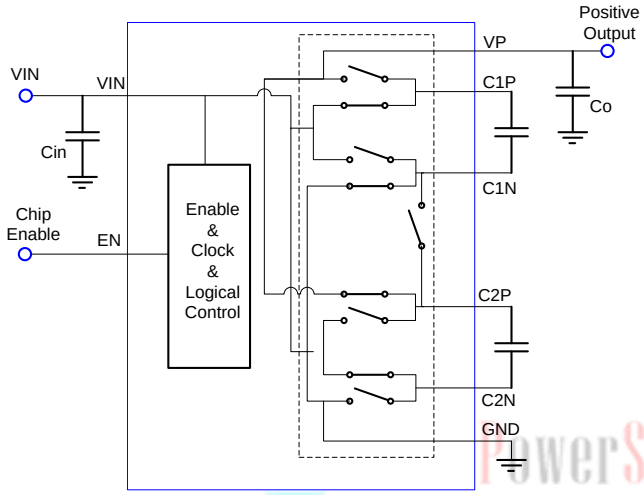


Figure 1. Positive Charge Pump Functional Block Diagram

The LP3102 positive charge pump provides an output voltage V_P of 1.5x or 2x the input voltage. The positive charge pump uses two external flying capacitors to generate the required output voltage. For the selected output to input ratio, the charge pump will configure the internal switches to charge the flying capacitors. Figure 1shows the functional diagram of the positive charge pump.

Negative Charge Pump Controller

The negative charge pump uses one external flying capacitor to generate an inverted negative voltage that is –1x of V_P. Figure 2 shows the functional block diagram of the negative charge pump.

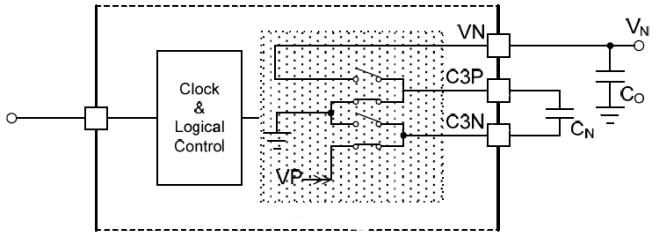


Figure 2. Negative Charge Pump Functional Block Diagram

LAYOUT CONSIDERATION

Use a ground plane for the LP3102 device that can be connected to the device expose pad and ground pin for optimal thermal characteristics.

Bypass Capacitors

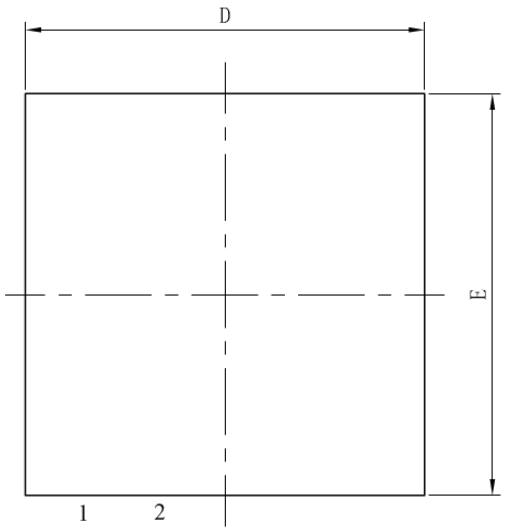
Place VIN, VP, and VN bypass capacitors as close as possible to the device pin. Keep the ground traces from the bypass to the ground plane as short as possible.

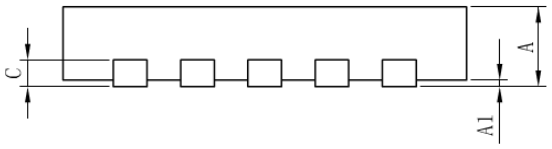
Flying Capacitors

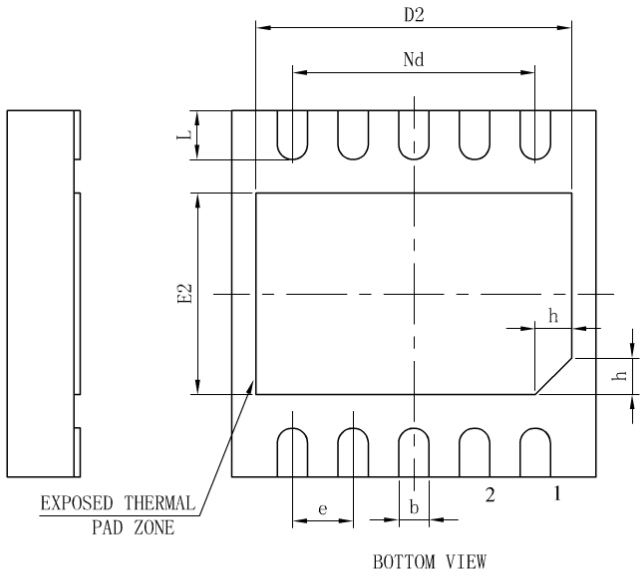
Place the flying capacitors as close to the device pins as possible to minimize trace noise since the flying capacitors to the pins will generate high transient voltage (dv/dt) switching signals

Packaging Information

TDFN-10







SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0. 70	0.75	0. 80
A1	—	0.02	0. 05
b	0. 18	0.25	0. 30
c	0. 18	0.20	0. 25
D	2. 90	3. 00	3. 10
D2	2. 40	2. 50	2. 60
e	0. 50BSC		
Nd	2. 00BSC		
E	2. 90	3. 00	3. 10
E2	1. 45	1. 55	1. 65
L	0. 30	0.40	0. 50
h	0. 20	0. 25	0. 30